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Patentanmeldung Nr. Patent application No. Demande de brevet n°

02078531.7

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Anmeldung Nr:
Application no.: 02078531.7
Demande no:

Anmeldetag:
Date of filing: 28.08.02
Date de dépôt:

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Method for reducing power consumotion in a state retaining circuit, circuit and layout therefore

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

G11C/

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR

Method for Reducing Power Consumption in a State Retaining Circuit, Circuit and Layout therefore

The present invention relates to a method, circuit and layout for reducing power consumption, in particular to a method, circuit and layout for reducing power consumption in a state retaining circuit during a standby mode.

Leakage power is increasingly becoming a large drain on battery operated devices, especially in a state retaining circuit having a large standby time. One obvious way to avoid leakage is to shut down the supply during standby. However, many systems have to maintain their state during standby and by shutting supply voltage in e.g. digital circuits, wherein the state is defined by the data stored in the latches or state retaining circuits, the state is lost.

US 5,812,463 provides a high speed, high voltage latch that reduces leakage current and vulnerability to latch-up. The latch has a switching transistor between a program power supply and the output. The switching transistor is turned off by the latch input when the latch input transitions so as drive the output to a low level. The switching transistor thereby reduces leakage current. An output driver transistor coupled to the program power supply is used. The latch output is initially pulled up through a Vcc power supply. The output driver transistor turns on after the latch output has been pulled up to an initial level. The output driver transistor then pulls up the output terminal to the high output voltage level through the program power supply. Pulling up the output initially with the Vcc power supply reduces the device power dissipation. The latch circuit further comprises two program power supplies to prevent latch-up, an n-well power supply and a local power supply. When the latch is switched from read mode to program mode the n-well power supply is raised to the program voltage before the local power supply is raised. When the latch is switched from program mode to read mode the n-well power supply voltage is not reduced until after the local power supply has been reduced and the rest of the circuit has discharged. This ensures the n-well voltage is at least as high as the voltage of the p-diffusions coupled to the n-well and thereby prevents latch-up. US 5812463 is related to a memory circuit. As an embodiment a low leakage latch circuit is proposed. The disclosed circuit is applicable to certain type of

memories like Flash or EEPROM. The proposed latch circuit is a level shifter which is used at the interface between normal and high voltage circuitry in flash memories.

US 5,955,913 discloses an integrated circuit selectively operable in either a first mode (consuming low power) or a second mode (consuming relatively high power). The circuit includes MOS transistors and a supply voltage circuit for at least one of the transistors. In both modes, the supply voltage circuit holds the body of each transistor at a fixed voltage (e.g., a voltage Vcc in a range from 5 to 5.5 volts, where each transistor is a PMOS device). In the second mode the supply voltage circuit supplies this fixed voltage to the source of each transistor, but in the first mode it supplies a voltage equal to or slightly offset from the fixed voltage to the source of each transistor. In some embodiments, the supply voltage circuit (in the first mode, after an initial transient state) supplies a first voltage to a well shared by a plurality of PMOS transistors, and a second voltage to the source of each PMOS device. Alternatively, the supply voltage circuit (in the first mode, after an initial transient state) supplies a first voltage to the body of each of a plurality of NMOS transistors, and a second voltage to the source of each NMOS device. The second voltage is preferably offset from the first voltage by a voltage drop chosen to achieve a desired decrease in transistor leakage current in the first mode and a desired power up time for a transition from the first mode to the second mode. In preferred embodiments, the integrated circuit is a memory chip including a flash memory array, the voltage drop is in the range from 1.4 volts to 2 volts, and the voltage drop is implemented with one diode-connected MOS transistor or two diode-connected MOS transistors connected in series.

US 2001/0038552 A1 discloses a semiconductor memory with static memory cells having an n-well in which PMOS transistors are formed and a p-well in which NMOS transistors are formed. The n- and p-wells are divided into blocks each containing a given number of memory cells. The n- and p-wells in each block receive voltages that vary depending on whether or not the memory cells are selected. If the memory cells are selected to operate, the threshold voltage of each transistor in the memory cells is decreased to increase current to be taken out of the memory cells. If the memory cells are not selected, the threshold voltage is increased to reduce leakage current of the memory cells. This arrangement suppresses standby current and improves the operation speed of the memory cells.

US 5955913 and US 2001/0038552 propose the classical idea of reducing leakage by electrically increasing the threshold voltage of the MOS switch using back-bias voltage. They give respective memory circuits as embodiments.

US 6,344,761 B2 discloses that in a current comparison type latch, during a reset mode of the current comparison type latch where the clock signal is at the "L" level, transistors which are disposed along the current path extending from the high potential power supply line to the low potential power supply line are turned OFF while transistors which connect the high potential power supply line to two output terminals are turned ON, so as to bring the potential of each of the two output terminals to a logic level (the "H" level or the "L" level), thereby preventing a through current from flowing from the high potential power supply line to the low potential power supply line. Therefore, a high-speed and high-precision current comparison is made while reducing the through current during a reset mode. US 6334761 B2 describes a current comparison type latch for use in an analog-digital converter and the like. The object is to provide a current comparison type latch which eliminates the through current flowing in a reset state so as to achieve a reduction in the power consumption, and which is capable of making a high-speed and high-precision comparison.

US 2002/0024873 A1 discloses a level converter converting a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential Vcc and a ground potential GND, into mutually complementary logic signals WD and ZWD of a high voltage Vpp and a negative potential Vbb. An RX decoder decodes an address signal to output a signal of an amplitude of (Vpp-Vbb) specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The non-selected word line receives negative potential Vbb from a word driver. The selected word line receives high voltage Vpp from the word driver. It is possible to suppress a channel leak current at a memory transistor in the non-selected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved. US 2002/0024873 discloses a dynamic semiconductor memory device storing information in the form of electrical charges. This memory comprises a structure for improving charge retention characteristics of memory cells.

US 6344761 and US 2002/0024873 relate to semiconductor memory devices with reduced leakage current and include the following features. When the low potential power source is switched off, transistors connected to a high potential source are switched on, preventing a through current. A separate power source is provided for NMOS devices.

It is an object of the present invention to provide a method, a circuit and a layout having improved power consumption characteristics in a state retaining circuit during a standby mode.

To achieve the object of the present invention a method for reducing the power consumption in a state retaining circuit during a standby mode is disclosed comprising, in an active state, providing a regular power supply VDD and a standby power supply VDD-STANDBY to the state retaining circuit; for a transition from an active state to a standby state, decreasing the regular power supply to ground level and maintaining the standby power supply VDD-STANDBY thus providing the circuit elements with enough power for retaining the state during standby mode; and for a transition from the standby state to the active state, increasing the regular power supply VDD from its ground level to its active level. The method allows to shut the regular supply to the digital circuits without losing the state of the circuit, thereby reducing leakage by a factor of about 100.

According to a preferred embodiment of the invention, the standby power supply VDD_STANDBY is decreased to a lower level which is enough for retaining the state of the circuit elements in moving from an active state to a standby state; and the standby power supply VDD_STANDBY is increased from its lower voltage to its active level in returning back into the active mode. The decreasing of the standby power supply VDD_STANDBY to a lower level reduces leakage power in a standby mode.

According to a preferred embodiment of the invention, retaining of the state of the circuit elements during standby mode is done by transistors with high threshold voltages. The use of transistors with high threshold voltage leads to a very small leakage power.

According to a preferred embodiment of the invention, a clock signal is held during standby mode.

To achieve the object of the present invention a circuit for reducing the power consumption in a state retaining circuit during a standby mode is disclosed comprising a clock unit providing at least one clock signal; a data input unit providing at least one input signal; a data output unit providing at least one output signal; a state holding circuit comprising circuit elements holding the state of the circuit during an a standby mode; a regular power supply supplying power to the circuit elements during an active mode; a standby power supply supplying power to the circuit elements during the active mode and the standby mode. The circuit for reducing the power consumption in a stage retaining circuit

during a standby mode reduces the power consumption by a factor of 100 in comparison to commonly used circuits for reducing power.

According to a preferred embodiment of the invention, the clock unit is connected to the regular power supply and to the standby power supply. The clock signal is maintained during a standby mode because of the connection of the clock unit to the standby power supply.

According to a preferred embodiment of the invention, the clock unit comprises at least one input terminal receiving a clock input signal and at least one clock output terminal. The clock unit is able to deal with at least one clock input signal and is able to put out at least one output clock signal. This is advantageous because different input clock signals can be used. The different output terminals can be connected to different circuit elements with different clock signals.

According to a preferred embodiment of the invention, the clock unit comprises at least one state retaining switch for retaining the state during a standby mode. It is an advantageous feature of the clock unit that every clock unit comprises at least one state retaining switch for retaining the state during a standby mode because the state is retained directly at the source of the clock signal.

According to a preferred embodiment of the invention, the clock unit comprises at least two inverter stages providing at least one inverted clock signal and at least one not inverted clock signal.

According to a preferred embodiment of the invention, the inverter stage comprises at least two transistors with different polarity.

According to a preferred embodiment of the invention, the data input unit is connected to the regular power supply.

According to a preferred embodiment of the invention, the data input unit comprises at least one input terminal receiving a data input signal and at least one output terminal.

According to a preferred embodiment of the invention, the data input unit is connected to the clock signal.

According to a preferred embodiment of the invention, the state holding unit is connected to the regular power supply and to the standby power supply.

According to a preferred embodiment of the invention, the state holding unit is connected to the inverted clock signal and to the not inverted clock signal.

According to a preferred embodiment of the invention, the state holding unit comprises at least one state retaining switch retaining the inverted data input signal and at least one state retaining switch retaining the not inverted data input signal.

According to a preferred embodiment of the invention, the state holding unit comprises a state retaining switch retaining the not inverted data input signal.

According to a preferred embodiment of the invention, the inverter stage comprises at least two transistors with opposite polarity.

According to a preferred embodiment of the invention, the state holding unit comprises a serial circuit for retaining the inverted data input signal.

According to a preferred embodiment of the invention, the serial circuit for retaining the inverted data input signal comprises a state retaining switch retaining the inverted data input signal connected to the standby power supply and a state retaining switch connected to the clock signal.

According to a preferred embodiment of the invention, the data output unit is connected to the regular power supply.

According to a preferred embodiment of the invention, the data output unit comprises at least one input terminal receiving a signal from the state holding unit, and at least one output terminal outputting the received signal from the state holding unit.

According to a preferred embodiment of the invention, the data output unit comprises at least one inverter stage.

According to a preferred embodiment of the invention, the inverter stage comprises at least two transistors with opposite polarity.

According to a preferred embodiment of the invention, the state retaining switch in the state holding circuit is a transistor with a high threshold voltage. The advantage of a transistor with a high threshold voltage is that the leakage power is very small.

According to a preferred embodiment of the invention, the circuit elements of the state retaining switch have a higher threshold voltage than the other circuit elements.

To achieve the object of the present invention a layout for reducing the power consumption and retaining the state of a circuit during standby mode is disclosed comprising a clock unit providing at least one clock signal; a data input unit providing at least one input signal; a data output unit providing at least one output signal; a state holding circuit comprising circuit elements holding the state of the circuit during a standby mode; a regular power supply supplying power to the circuit elements during an active mode; and a standby

power supply supplying power to the circuit elements during the active mode and the standby mode.

According to a preferred embodiment of the invention, the clock unit comprises at least one state retaining switch which is a PMOS device.

According to a preferred embodiment of the invention, the state holding circuit comprises an inverter stage receiving and inverting the data input signal and comprising at least one PMOS device.

According to a preferred embodiment of the invention, the state holding circuit comprises a serial circuit for retaining the inverted data input signal connected to the inverter stage and comprising at least one PMOS device.

According to a preferred embodiment of the invention, the circuit elements are PMOS and/or NMOS devices.

According to a preferred embodiment of the invention, the PMOS device is provided in a separate N-well.

According to a preferred embodiment of the invention, the separate N-well is connected to the standby power supply.

The separate N-well is connected to the standby power supply in order to avoid junctions getting forward biased during standby.

These and various other advantages and features of novelty which characterize the present invention are pointed out with particularity in the claims annexed hereto and forming a part hereof. However, for a better understanding of the invention, its advantages, and the object obtained by its use, reference should be made to the drawing which forms a further part hereof, and to the accompanying descriptive matter in which there is illustrated and described a preferred embodiment of the present invention.

Figure 1 shows an exemplary schematic circuit diagram of the present invention.

The circuit diagram of Figure 1 comprises FETs with a p-channel and an n-channel. A FET with a p-channel is on when the voltage between the gate and the source

terminal is smaller than zero and is off when the voltage between the gate terminal and the source terminal is greater than zero. A FET is on when the voltage between the gate terminal and the source terminal is greater than zero and is off when the voltage between the gate and source terminals is smaller than zero.

The circuit diagram shows a clock unit 1 comprising an input terminal 2 connected to a gate contact 4 of a transistor 36 and to a gate contact 12 of a transistor 38. The transistor 36 is a FET with a p-channel and transistor 38 is a FET with an n-channel. A source terminal 6 and a base terminal 7 of transistor 36 are connected to a standby power supply VDD_standby. A drain terminal 8 of transistor 36 is connected to a drain terminal 10 of transistor 38. A source terminal 14 of transistor 38 is connected to ground. Transistor 38 is a transistor with a high threshold voltage. This is shown by the two letters Vt.

All other transistors, which are transistors with a high threshold voltage, are marked with the same letters. The transistors 36 and 38 form an inverter stage. An inverted clock signal CKPNI of terminal 2 is output at the drain terminals 8 and 10. Transistor 36 retains the inverted clock signal CKPNI during the standby mode. The drain terminals 8 and 10 are connected to a gate contact 22 of a p-channel transistor 40 and to a gate contact 30 of an n-channel transistor 42. A source terminal 24 of transistor 40 is connected to the regular power supply VDD and a base terminal 25 is connected to VDD_STANDBY. A drain terminal 26 of transistor 40 is connected to a drain terminal 28 of transistor 42. A source terminal 32 of transistor 42 is connected to ground.

The two transistors 40 and 42 form another inverter stage. This inverter stage inverts the inverted clock signal CKPNI into the not inverted clock signal CKPI. The not inverted clock signal CKPI is provided at terminal 34. Terminal 34 is connected to the drain terminals 26 and 28.

Figure 1 shows also a data input unit 3. The data input unit 3 comprises an input terminal 50 connected to a gate contact 52 of a p-channel transistor 70 and to a gate contact 66 of an n-channel transistor 75. A source terminal 54 of transistor 70 is connected to the regular power supply VDD. A base terminal 55 of transistor 70 is connected to VDD_STANDBY. A drain terminal 56 of transistor 70 is connected to a source terminal of a p-channel transistor 72 at node 56. A gate terminal 58 of transistor 72 is connected to the inverted clock signal CKPNI. A base terminal 71 of transistor 72 is connected to VDD_STANDBY. A drain contact of transistor 72 is connected to a drain contact of an n-channel transistor 74 at node 60. A gate terminal 62 of transistor 74 is connected to the not inverted clock signal CKPI. A source terminal of transistor 74 is connected to a drain

terminal of an n-channel transistor 75 at node 64. A source terminal of transistor 75 is connected to ground at node 68. The input signal is supplied to a state holding circuit at node 60.

The state holding circuit 5 comprises a p-channel transistor 142 connected at its gate 128 to node 60. A source terminal 130 of transistor 142 is connected to the VDD_STANDBY. A drain terminal 132 of transistor 142 is connected to a drain terminal 122 of an n-channel transistor 144. A gate terminal 124 of transistor 144 is also connected to the node 60. A source terminal 126 is connected to ground. The transistors 142 and 144 form an inverter stage. As mentioned before, the transistors 142 and 144 are marked with the letters Vt, and are therefore transistors with a high threshold voltage. Transistor 142 retains an input signal in case of a standby mode. The drain contacts 132 and 122 represent the output of the inverter stage formed by the two transistors 142 and 144.

A signal S supplied at the drain terminals 132 and 122 represents the data input signal of terminal 50. The signal S is connected to a gate terminal 82 of a p-channel transistor 78. Transistor 78 is a transistor with a high threshold voltage. A base terminal 83 of transistor 78 is connected to VDD_STANDBY. A gate terminal 88 of a p-channel transistor 85 is connected to the not inverted clock signal CKPI. A base terminal 87 of transistor 85 is connected to VDD_STANDBY. A source terminal 80 of transistor 78 is connected to the standby power supply VDD_STANDBY. A drain contact 84 of transistor 78 is connected to a source terminal 86 of transistor 85. A gate terminal 106 of transistor 138 is connected to the inverted clock signal CKPNI. A drain terminal 104 of transistor 138 is connected to terminal 90 of transistor 85. A source terminal 108 of transistor 138 is connected to a drain terminal 110 of an n-channel transistor 140. A source terminal 114 of transistor 140 is connected to ground. A gate terminal 112 of transistor 140 is connected to the signal S. Transistor 140 is a transistor with a high threshold voltage.

An inverted signal SN is provided at the drain terminal 90. This inverted signal SN is supplied to a data output unit 7. The data output unit 7 receives the inverted signal SN at a gate terminal 150 of p-channel transistor 162 and at a gate terminal 160 of an n-channel transistor 164. A source terminal 152 of transistor 162 is connected to the regular power supply VDD. A base terminal 153 of transistor 162 is connected to VDD_STANDBY. A drain terminal 154 of transistor 162 is connected to a drain terminal 156 of transistor 164 and to a data output terminal 166. A source terminal 158 of transistor 164 is connected to ground. The transistors 162 and 164 form an inverter stage.

The present circuit comprises latches, the states of which latches need to be retained during standby - called state holding latches-, and combinatorial logic, latches etc. whose states need not be retained. Two supplies are used: one is the regular supply (VDD) and the other one is a standby supply (VDD_STANDBY). VDD is supplied to circuits the state of which is not retained whereas state holding latches are supplied with both the VDD and VDD_STANDBY. During active operation, both supplies are on.

To go into standby, the VDD is reduced to ground level and VDD_STANDBY is reduced to a lower voltage, which is just enough to keep the state in the state holding latches. Thus except for state holding latches, there is no standby leakage. The standby supply VDD_STANDBY provides the necessary current to maintain the state in the state holding latches. As very small current is drawn from VDD_STANDBY during the active and standby mode, routing requirements of VDD_STANDBY are relaxed.

The operation of the circuit of Fig. 1 is as follows. First, consider active mode, where both VDD and VDD_STANDBY are on. If the CLOCK is high, DATAIN determines the states of nodes S and SN. When CLOCK goes low, the feedback loop in the state holding latch is complete, and the previous states of nodes S and SN is maintained. Now to move into standby, the normal supply VDD is lowered to ground level and then VDD_STANDBY is reduced to a lower level (just enough to maintain the state). As VDD is lowered, CLOCK remains at ground level and the switches 36 - 85 maintain the states of nodes S, SN, CKPNI and CKPI.

The voltage of the rest of the nodes reach ground level and they become floating. Thus during standby, there is only a small leakage due to switches getting VDD_STANDBY. This small leakage is further reduced by making these switches high Vt as shown in Fig 1. Now to return back into active mode, VDD_STANDBY is raised to its active level, and then VDD is raised from the ground level back to its active level. The state of CLOCK is held during standby by outside circuitry and thus CLOCK remains low. The topology of the circuit is such that the states of nodes CKPNI, CKPI, S, and SN are maintained. The circuit can now begin its active operation.

All the P-switches in the latch are placed in an N-well, which is connected to supply VDD_STANDBY. This avoids the source/drain junctions of PMOS transistors getting forward biased during standby mode.

The invention allows to shut down the regular supply to the digital circuits without loosing the state of the circuit, thereby reducing leakage by a factor of approximately 100. The state holding latch uses high Vt switches, and therefore its leakage is very small. In

a digital circuit that uses this scheme, the logic gates can be optimized for speed by using low Vt switches without the cost of high standby leakage as the supply for the logic can be turned off during standby. Thus, this scheme offers high-performance and low leakage.

The present invention is applicable for all devices, which require low standby leakage and standby state retention; especially the battery powered devices.

New characteristics and advantages of the invention covered by this document have been set forth in the foregoing description. It will be understood, however, that this disclosure is, in many respects, only illustrative. Changes may be made in details, particularly in matters of shape, size, and arrangement of parts, without exceeding the scope of the invention. The scope of the invention is, of course, defined in the language in which the appended claims are expressed.

CLAIMS:

1. A method for reducing the power consumption in a state retaining circuit during a standby mode, comprising:

in an active state, providing a regular power supply and a standby power supply to the state retaining circuit;

for a transition from an active state to a standby state, decreasing the regular power supply to ground level and maintaining the standby power supply thus providing the circuit elements with enough power for retaining the state during standby mode; and

for a transition from the standby state to the active state, increasing the regular power supply from its ground level to its active level.

2. The method of claim 1, wherein the standby power supply is decreased to a lower level which is enough for retaining the state of the circuit elements in moving from an active state to a standby state; and the standby power supply is increased from its lower voltage to its active level in returning back into the active mode.

3. The method of claim 2, wherein retaining of the state of the circuit elements during standby mode is done by transistors with high threshold voltages.

4. The method of claim 1, wherein a clock signal is held during standby mode.

5. A circuit for reducing the power consumption in a state retaining circuit during a standby mode, comprising:

a clock unit for providing at least one clock signal;

a data input unit for providing at least one input signal;

a data output unit for providing at least one output signal;

a state holding circuit comprising circuit elements for holding the state of the circuit during an a standby mode;

a regular power supply for supplying power to the circuit elements during an active mode;

a standby power supply for supplying power to the circuit elements during the active mode and the standby mode.

6. The circuit of claim 5, wherein the clock unit is connected to the regular power supply and to the standby power supply.

7. The circuit of claim 5, wherein the data input unit is connected to the regular power supply.

8. The circuit of claim 5, wherein the data input unit is connected to the clock signal.

9. The circuit of claim 5, wherein the state holding unit is connected to the regular power supply and to the standby power supply.

10. The circuit of claim 5 or 9, wherein the state holding unit comprises a serial circuit for retaining the inverted data input signal.

11. The circuit of claim 5, wherein the data output unit comprises at least one input terminal for receiving a signal from the state holding unit, and at least one output terminal for outputting the received signal from the state holding unit.

12. The circuit of any of the claims 5 to 11, wherein the circuit elements of the state retaining switch have a higher threshold voltage than the other circuit elements.

13. A layout for reducing the power consumption and retaining the state of a circuit during standby mode, comprising:

a clock unit for providing at least one clock signal;

a data input unit for providing at least one input signal;

a data output unit for providing at least one output signal;

a state holding circuit comprising circuit elements for holding the state of the circuit during a standby mode;

a regular power supply for supplying power to the circuit elements during an active mode; and

a standby power supply for supplying power to the circuit elements during the active mode and the standby mode.

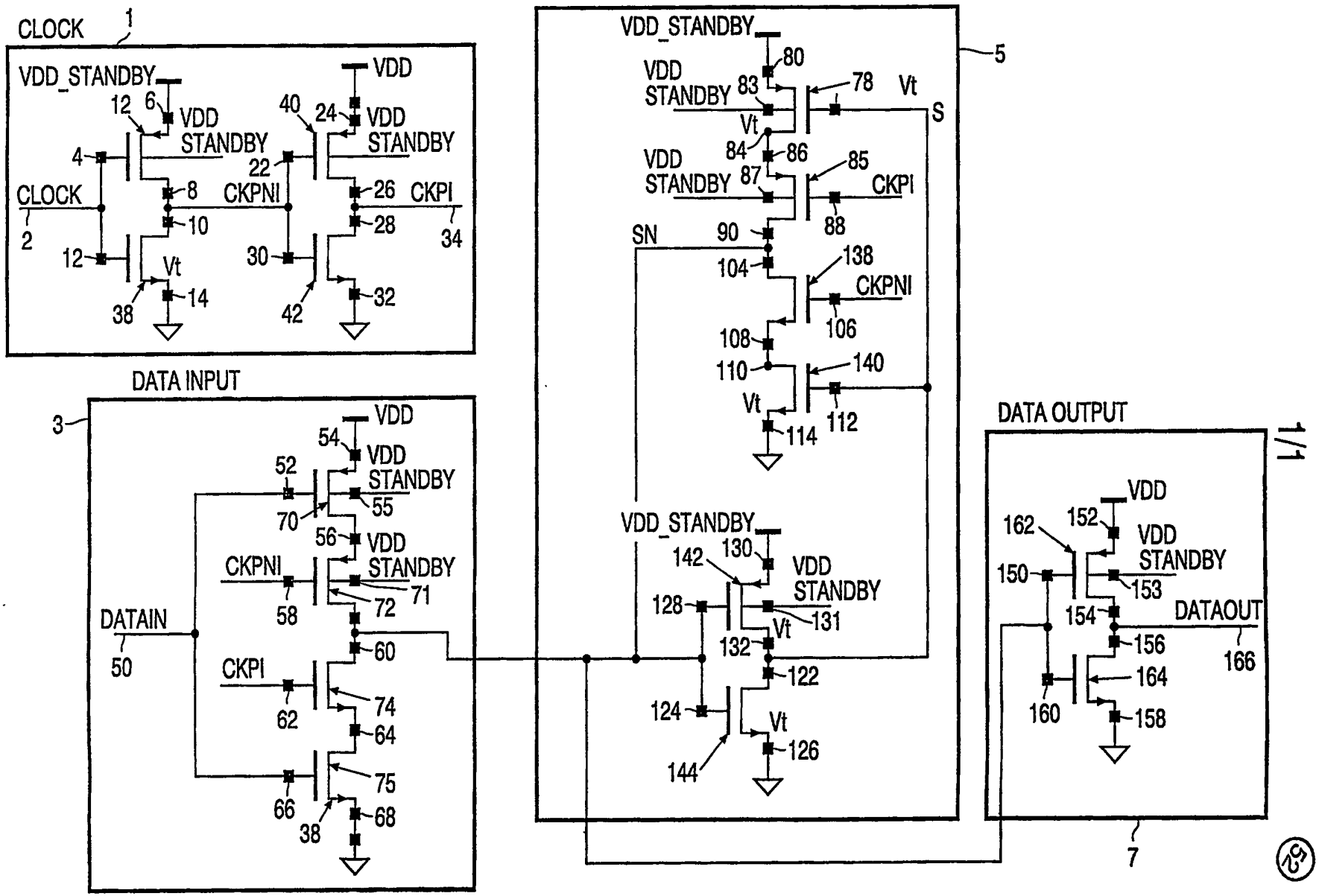
14. The layout of claim 13, wherein the circuit elements are PMOS and/or NMOS devices.

15. The layout of claim 13 or 14, wherein the PMOS device is provided in a separate N-well which is connected to the standby power supply.

ABSTRACT:

A method for reducing the power consumption in a state retaining circuit during a standby mode is disclosed comprising, in an active state, providing a regular power supply (VDD) and a standby power supply (VDD_STANDBY) to the state retaining circuit; for a transition from an active state to a standby state, decreasing the regular power supply to ground level and maintaining the standby power supply (VDD_STANDBY) thus providing the circuit elements (36, 142, 78, 85) with enough power for retaining the state during standby mode; and for a transition from the standby state to the active state, increasing the regular power supply (VDD) from its ground level to its active level. A circuit for reducing the power consumption in a state retaining circuit during a standby mode is disclosed comprising a clock unit (1) providing at least one clock signal; a data input unit (3) providing at least one input signal; a data output unit (7) providing at least one output signal; a state holding circuit comprising circuit elements (36, 142, 78, 85) holding the state of the circuit during an a standby mode; a regular power supply supplying power to the circuit elements during an active mode; a standby power supply supplying power to the circuit elements (36, 142, 78, 85) during the active mode and the standby mode. A layout for reducing the power consumption and retaining the state of a circuit is also disclosed.

Fig. 1



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